# POWER AMPLIFIER FOR MICROWAVE DIGITAL
# RADIOS WITH INHERENT PHASE COMPENSATION

P. BURA   D. GELERMAN   P. NTAKE

NORTHERN TELECOM, TRANSMISSION NETWORKS DIV.
ST. LAURENT, P.Q., CANADA

## ABSTRACT

The linearity requirements and the design of an amplifier for a 64 QAM digital radio are described. A partial phase compensation between the cascaded bi-polar transistor and FET amplifying stages helps to achieve bit error rates better than $10^{-20}$.

## 64 QAM CONSTELLATION
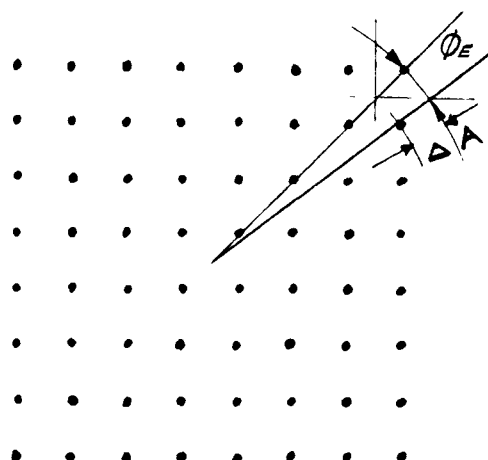


## PERFORMANCE REQUIREMENTS

The 64 QAM modulation,which consists of a constellation of 64 discrete states with the difference between the neighboring states as low as 1.2 dB in power level and 9.5° in phase, imposes severe linearity requirements for the system as a whole and for the PA in particular. In order to meet the field requirement (per hop) of $10^{-15}$ bit error rate (BER) thetransmitter-receiver bay specification calls for $10^{-20}$ BER or less than 8% eye closure. Fig.1 shows how the eye closure and intermodulation ratio (IMR) requirement translates into the maximum allowed phase or gain change. Thus, in order to meet the BER requirement, the PA must have less than 0.6°

phase change (at zero gain compression) and less than 0.1 dB gain compression (or expansion) with zero phase change. The corresponding IMR requirement is 38dBc at the peak level. For a PA with an output level of 28 dBm RMS, the peak state is at 31.7 dBm and with the filter over-shoot this can be as high as 32.8  dBm. Thus, an amplifier with a third order intercept as high as 52 dBm may be required. A 3.7-4.2 GHZ amplifier was designed to meet the linearity requirements. It uses bi-polar transistors (BPT) in the input module and FETs in the output for inherent phase compensation.

FIG.1  AMPLITUDE AND PHASE VS 3rd ORDER IMR
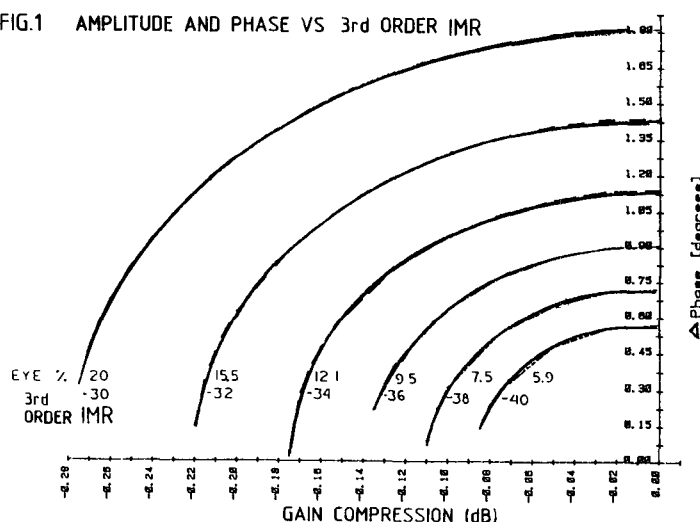


## DEVICE NON-LINEARITIES

Because of their excellent performance at microwave frequencies the devices used are Field-effect transistors (FET). Unfortunately, for historical reasons, the devices have been optimised for output power and efficiency, often with the sacrifice of linearity. This is especially noticable in the internally matched power FETs where, in addition to inherent non-linearity, it is often further enhanced by the matching circuit.

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In addition to FETs the bi-polar transistors are used. They operate satisfactorily at 4 GHz and offer several advantages over FETs at that frequency: lower cost, longer life, lower thermal resistance and easier matching (lower Q).

A) FET

The Schottky barrier gate capacitance Cg exhibits an approximate inverse square-root variation with the applied reverse voltage. When an RF voltage is applied the capacitance decrease during the negative half-cycle is smaller than the corresponding increase during the positive half-cycle: i.e. average Cg increases with RF drive. The change in the gm, the transconductance, is very similar, since the drain current depends directly on the channel opening, which is,in turn, determined by the gate depletion layer. Thus, with an RF drive, the average channel opening is slightly increased. Since the gain of an FET amplifier is proportional to (gm/Cg) , the increase in gm (with RF drive) tends to cancel out partially the increase in Cg. However, the RF drive has more effect on the amplifier phase. In addition to the effect on Cg and gm, the increased channel opening with the RF drive, shortens the effective length between the source and the drain. This slight shortening of the transit length results in decrease in the transit time, i.e. positive phase change. As RF drive power increases further, strong non-linear effects become predominant, viz. the "knee" of the Id-Vd characteristic and the forward conduction or reverse breakdown in the gate. The effect of these major non-linear effects is to make the phase change sharply negative.

B) Bi-polar Transistor

The two non-linear elements are: 1) current dependent $\beta$ and 2) voltage dependent collector capacitance Cc. Increasing base current decreases the value of $\beta$. Thus when RF drive is applied to the base, the increase in the collector current during the positive half-cycle is smaller than the decrease during the negative half-cycle i.e. the average collector current Ic tends to decrease with RF drive. The decreasing Ic increases the reverse voltage across the collector junction with a corresponding increase in the depletion layer width. The depletion layer transit time is increased and this causes the negative phase change in the amplifier. This is the opposite change to that of the FET amplifier. Thus, by cascading BPT and FET stages a partial phase change compensation will take place, i.e. the phase of a BPT/FET amplifier will remain constant over a wider range of output power level.

## 3.7 - 4.2 GHz PA

The PA, as shown in Fig. 2, consists of two modules. The input module, with maximum gain of 25dB consists of three BPT stages and a PIN diode for level adjustment and temperature compensation. The output module with 20 dB gain consists of two FET stages and a coupled detector circuit to feed the PIN drive for the temperature compensation. There are two output power options: 26.5 dBm (RMS) uses a 3w FET and 28.5 dBm (RMS) uses a 6w FET.

Fig.3 shows the output phase variation as the input power level is swept over 15dB range. The phase of the output stage only (3W FET) shows a change of + 1.4° at 33 dBm output level. With the BPT driver module included, the phase change at 33 dBm has been reduced to -0.3°.

Fig.4 shows the intermodulation ratio (IMR) as a function of the output level. It deviates from the ideal third order slope at 29dBm single carrier level.

Fig.5 shows the results of bit-error rate measurements both with and without pre-distortion. BER varies between $10^{-28}$ at the nominal PA output of 26 dBm and $10^{-16}$ at 29 dBm. The predistortion improves the BER over 26 to 29 dBm output power levels but looses its effectiveness at higher levels where the output FET deviates sharply from the third order behaviour. Pre-distortion circuit, shown in Fig.6, compensates for the non-linearities of the up-converter and the PA. A portion of the IF signal is passed through a "cuber" circuit. Its amplitude and phase is adjusted for best IMD or BER performance. It is then added to the main IF path and fed to the up-converter and then to PA.

CONCLUSIONS

A properly adjusted BPT-FET PA has an intercept point as high 49dBm with a 3w FET in the output stage. BER of $10^{-20}$ was measured at 28dBm (64 QAM RMS) with pre-distortion the output can be increased to 29.5 dBm.

REFERENCES

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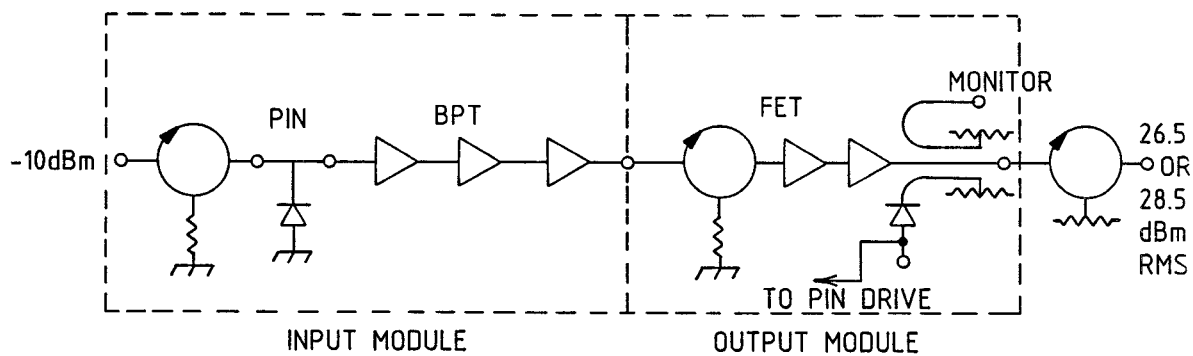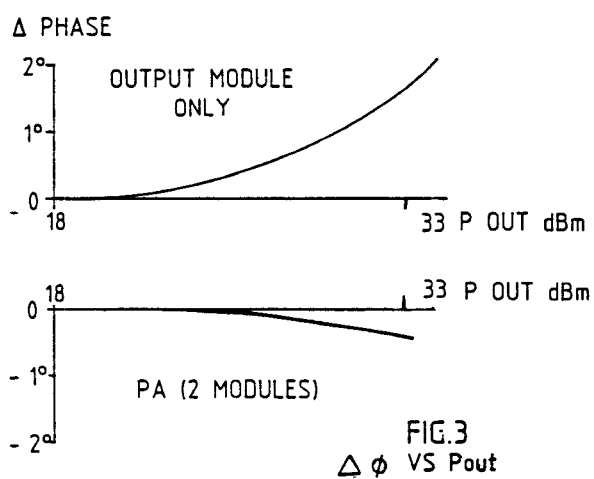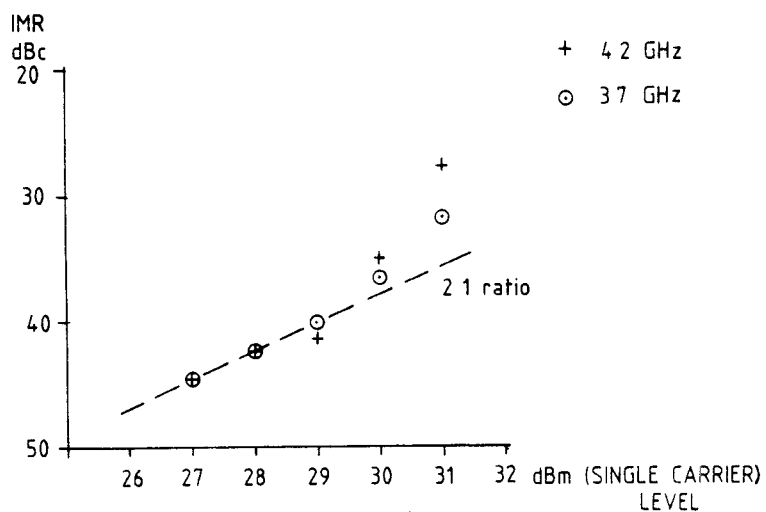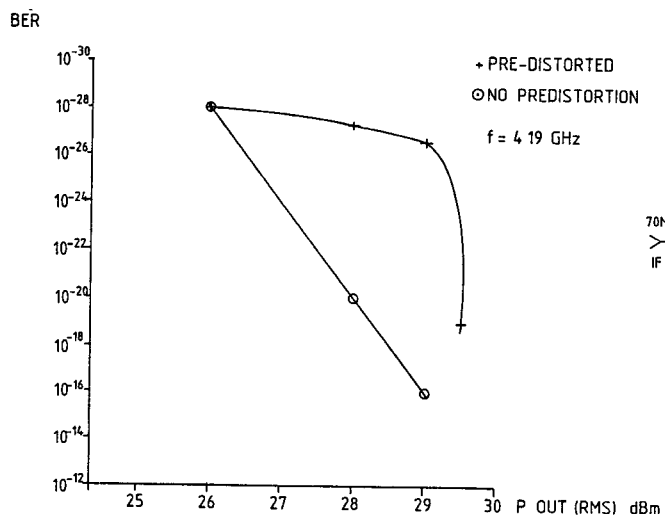
FIG.2
PA BLOCK DIAGRAM



FIG.3
Δ φ VS Pout



FIG.4
IMR VS P out



FIG 5
BER VS Pout



FIG.6
PREDISTORTION